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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/724,781	12/02/2003	Masashi Horiguchi	501.37021VV4	1908

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EXAMINER	
HO, HOAI V	
ART UNIT	PAPER NUMBER
2818	

DATE MAILED: 05/11/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

10/724,781

Applicant(s)

HORIGUCHI ET AL.

Examiner

Hoai V. Ho

Art Unit

2818

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 02 December 2003.
- 2a) ☐ This action is FINAL. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-5 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-5 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 02 December 2003 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☒ Certified copies of the priority documents have been received in Application No. 09/289,660.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date 12/03
- 4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date _____
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: _____

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1. This office acknowledges receipt of the following items from the Applicant:

Information Disclosure Statement (IDS) was considered.

Papers submitted under 35 U.S.C. 119(a)-(d) have been placed of record in the file.

2. Claims 1-5 are presented for examination.

Claim Rejections - 35 USC §102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

(e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) and the Intellectual Property and High Technology Technical Amendments Act of 2002 do not apply when the reference is a U.S. patent resulting directly or indirectly from an international application filed before November 29, 2000. Therefore, the prior art date of the reference is determined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

4. Claims 1-5 are rejected under 35 U.S.C. 102(e) as being anticipated by Fujioka U. S. Patent No. 5804893.


As per claims 1-3, Figure 5 of Fujioka is directed to a synchronous DRAM (col. 6, lines 27) comprising: a first input terminal which receives an external clock signal (CLK); a second


input terminal which receives a clock enable signal (CKE), a plurality of third input terminals which receive command signals (RE, CE W, CE), a fourth input terminal which receives an external power supply voltage (V_{cc} , fig. 6), and a voltage limiter circuit (51) which generates an internal power supply voltage lower than said external power supply voltage (col. 1, lines 17-20), and a control circuit (32 and 34) which receives said command signals in said external clock signal, synchronism with wherein said DRAM is in a power down mode (31) when said clock enable signal is low (col. 7, lines 9-22 and 215 of fig. 6), wherein said DRAM is out of said power down mode when said clock enable signal is high (col. 7, lines 9-22 and 215 of fig. 6), wherein said voltage limiter circuit (51, col. 8, lines 15-17) is not in operation when said DRAM is in said power down mode, and wherein said voltage limiter circuit is in operation (51, col. 8, lines 18-28) when said DRAM is out of said power down mode.

As per claims 4 and 5, Figure 5 of Fujioka is directed to a synchronous DRAM (col. 6, lines 27) comprising: a first power supply circuit (51) which receives an externally supplied voltage (V_{cc} , (col. 1, lines 17-20) and outputs an internal supply voltage (a line connects to 50, 51, 53,...) and a second power supply circuit (50) which receives said externally supplied voltage and outputs said internal supply voltage, wherein said synchronous DRAM operates in a power down mode and a mode (col. 3, lines 14-20), prior to said power down mode, in which said synchronous DRAM receives a clock signal and stands by for a power down mode command signal to begin said power down mode (col. 8, lines 15-28), wherein said first power supply circuit is not in operation when said semiconductor device is in said power down mode (col. 18, lines 15-17), and wherein said second power supply circuit is continuously in operation during said power down mode (col. 18, lines 18-28).

5. The prior art made of record and not relied upon is considered pertinent to applicants' disclosure. Oh (USP 8577652) discloses a voltage detecting circuit in a synchronous DRAM in Figures 1 and 4, abstract, col. 4, lines 34-37, col. 5, lines 10-20, col. 6, lines 20-26 and 47-51.
6. When responding to the office action, Applicants are advised to provide the examiner with the line numbers and page numbers in the application and/or references cited to assist the examiner to locate the appropriate paragraphs.
7. A shortened statutory period for response to this action is set to expire 3 (three) months and 0 (zero) day from the date of this letter. Failure to respond within the period for response will cause the application to become abandoned (see MPEP 710.02 (b)).
8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to whose telephone number is (571) 272-1777. Other inquiries of this application should be called to (571) 272-1562 or the fax number (703) 872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).


H. Ho
March 19, 2004


Hoai V. Ho
Primary Examiner
Art Unit 2818